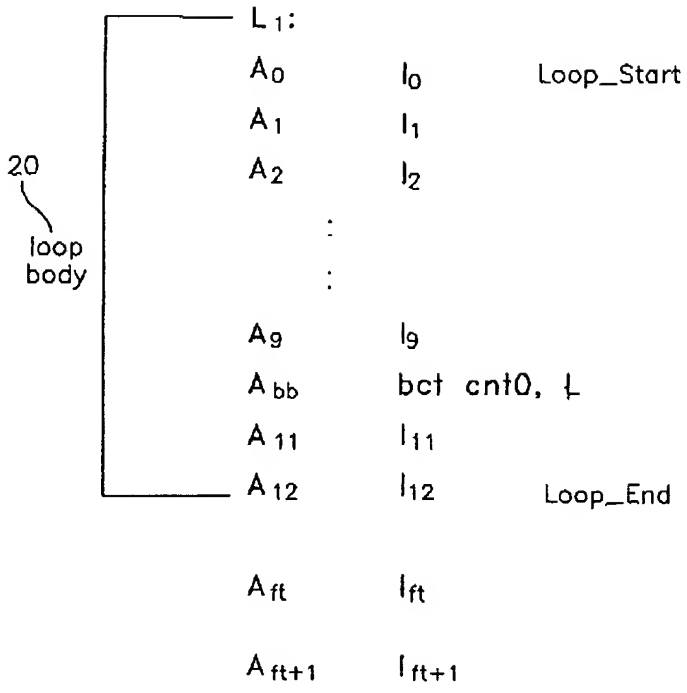
L 1:
A0 I0 Loop_Start
A1 I1
A2 I2
:
:
A9 I9
A bb bct cnt0, L
A 11 I11
A 12 I12 Loop_End
A ft I ft
A ft+1 I ft+1
20
loop
body

FIG. 1a

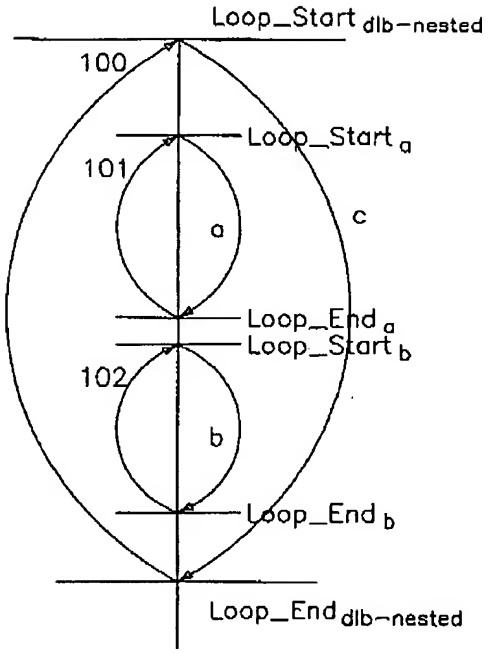

FIG. 1b

PAGE 19/24 * RCVD AT 6/13/2006 8:09:51 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/3 * DNIS:2738300 * CSID:19149453281 * DURATION (mm-ss):05-22

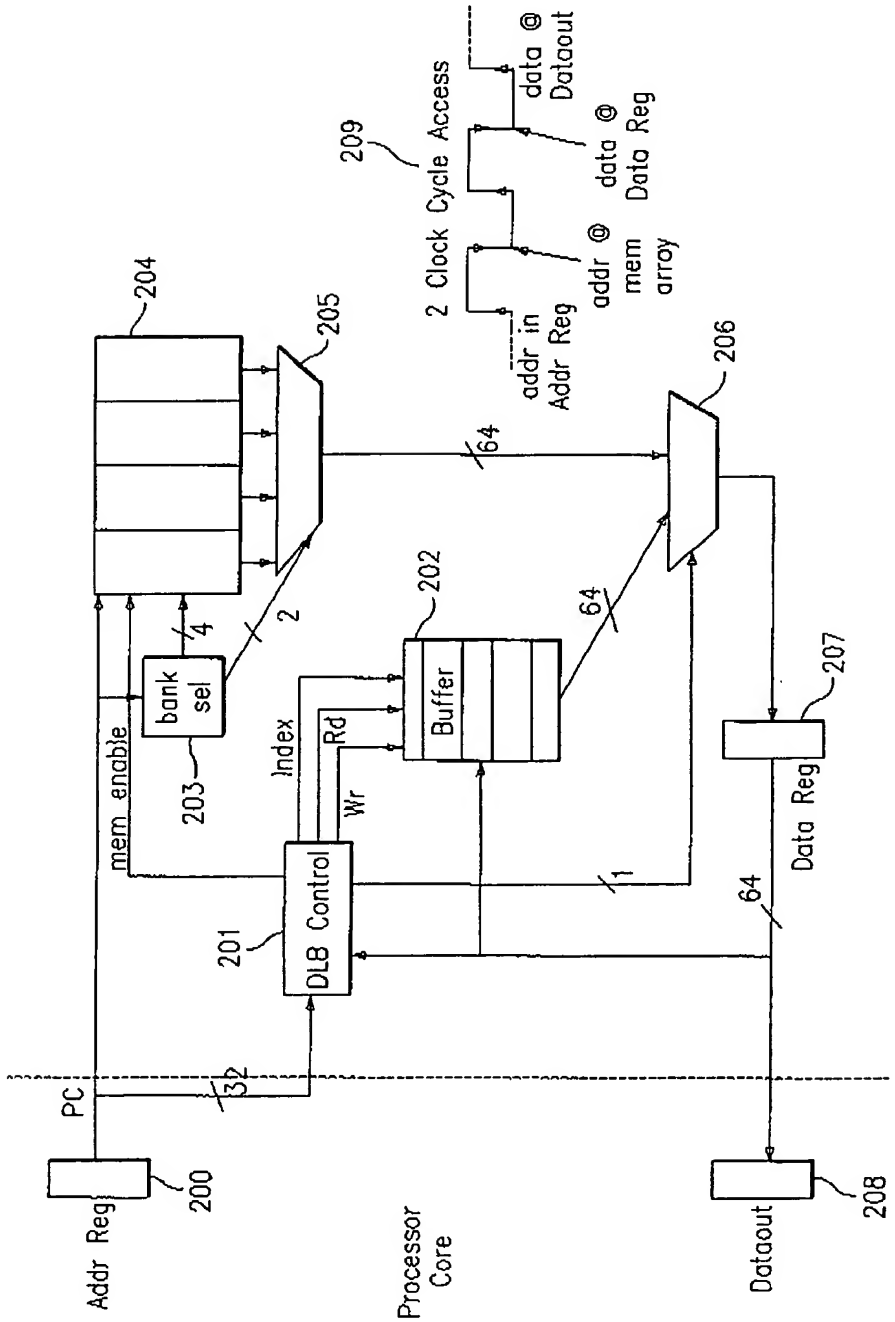
data @ Dataout
data @ Data Reg
addr @ mem array
addr in Addr Reg
2 Clock Cycle Access
209
204
205
206
64
202
Buffer
64
2
4
bank sel
203
mem enable
Index
Rd
Wr
207
Data Reg
64
1
DLB Control
201
32
PC
200
Addr Reg
Processor Core
Dataout
208

FIG. 2a

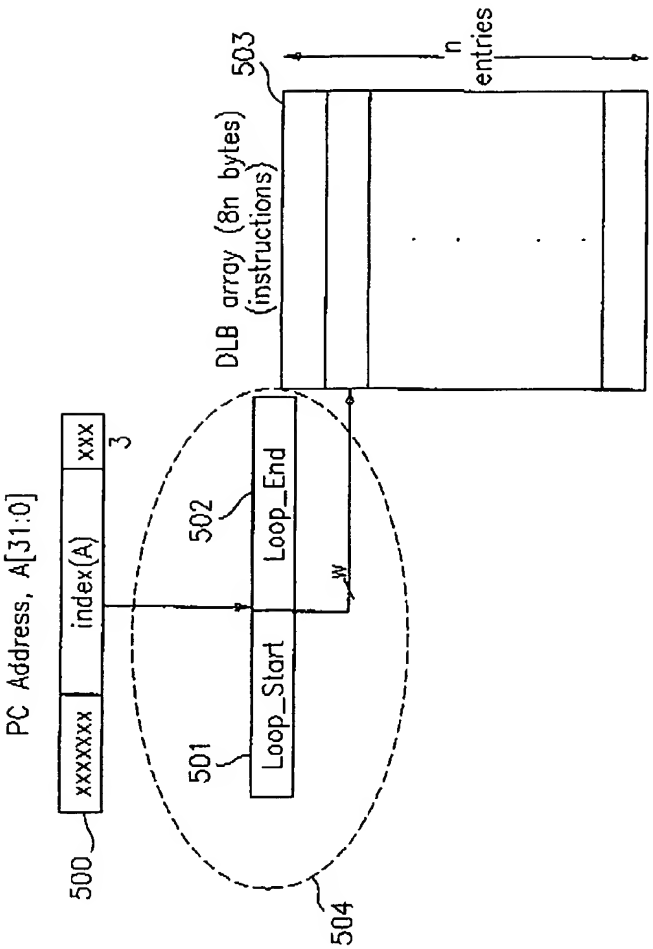
503
n
entries
DLB array (8n bytes)
(instructions)
PC Address, A[31:0]
xxxxxxx
index(A)
xxx
3
500
502
Loop_End
501
Loop_Start
w
504

FIG. 2b

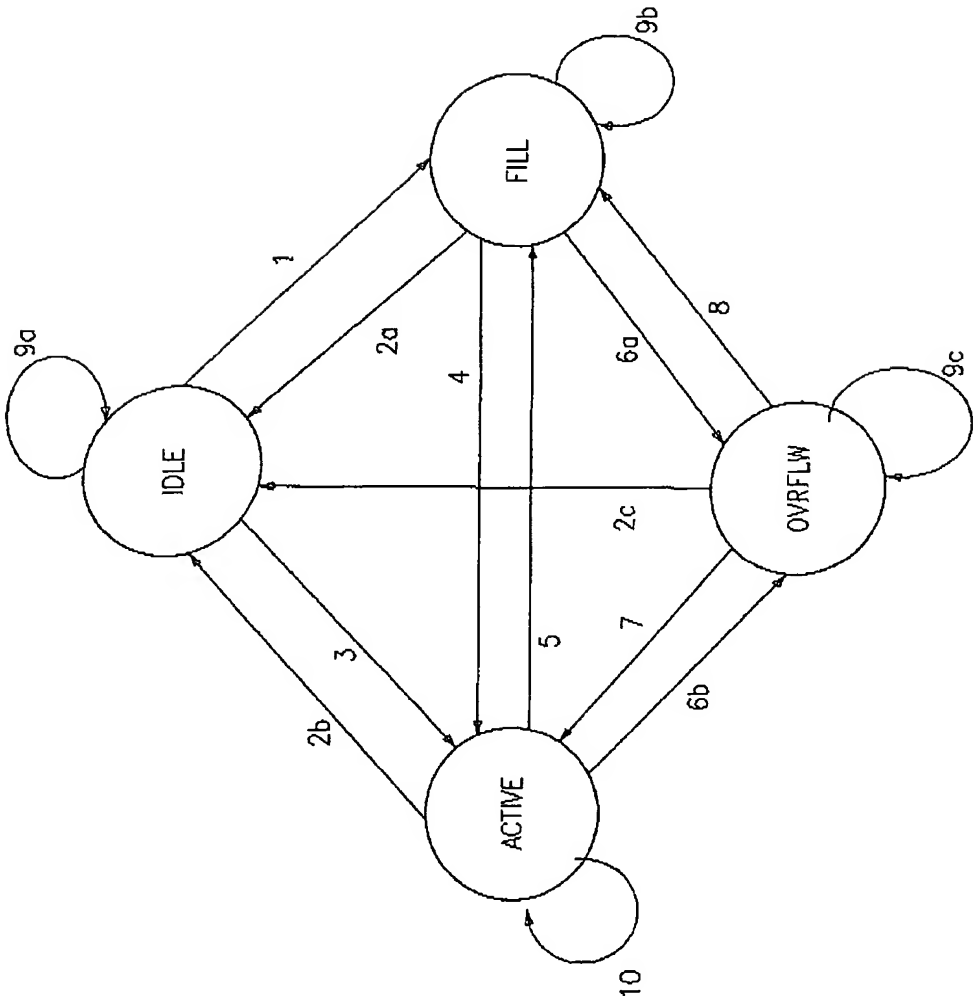

FIG. 3a

ID	From - To	Condition
1	I–F	[(backward branch (bb) detected & taken) || (move within loop range & entry invalid)]
2a 2b 2c	F–I A–I O–I	[(bb not taken) || (another cof causes move outside loop range)]
3	I–A	(move into loop range & entry valid)
4	F–A	[(bb is taken again) || (another indented bb is taken)] & (entry valid)
5	A–F	[(resume filling rest of loop) || (move within loop range & entry invalid)]
6a 6b	F–O A–O	(end of physical loop buffer reached)
7	O–A	[(cof caused within loop range) || (bb detected and taken again)] & [(next_data within buffer range) & (entry valid)]
8	O–F	[(cof caused within loop range) || (bb detected and taken again)] & [(next_data within buffer range) & (entry invalid)]
9a 9b 9c	I–I F–F O–O	(no cof)
10	A–A	(no cof) & (entry valid)

FIG. 3b

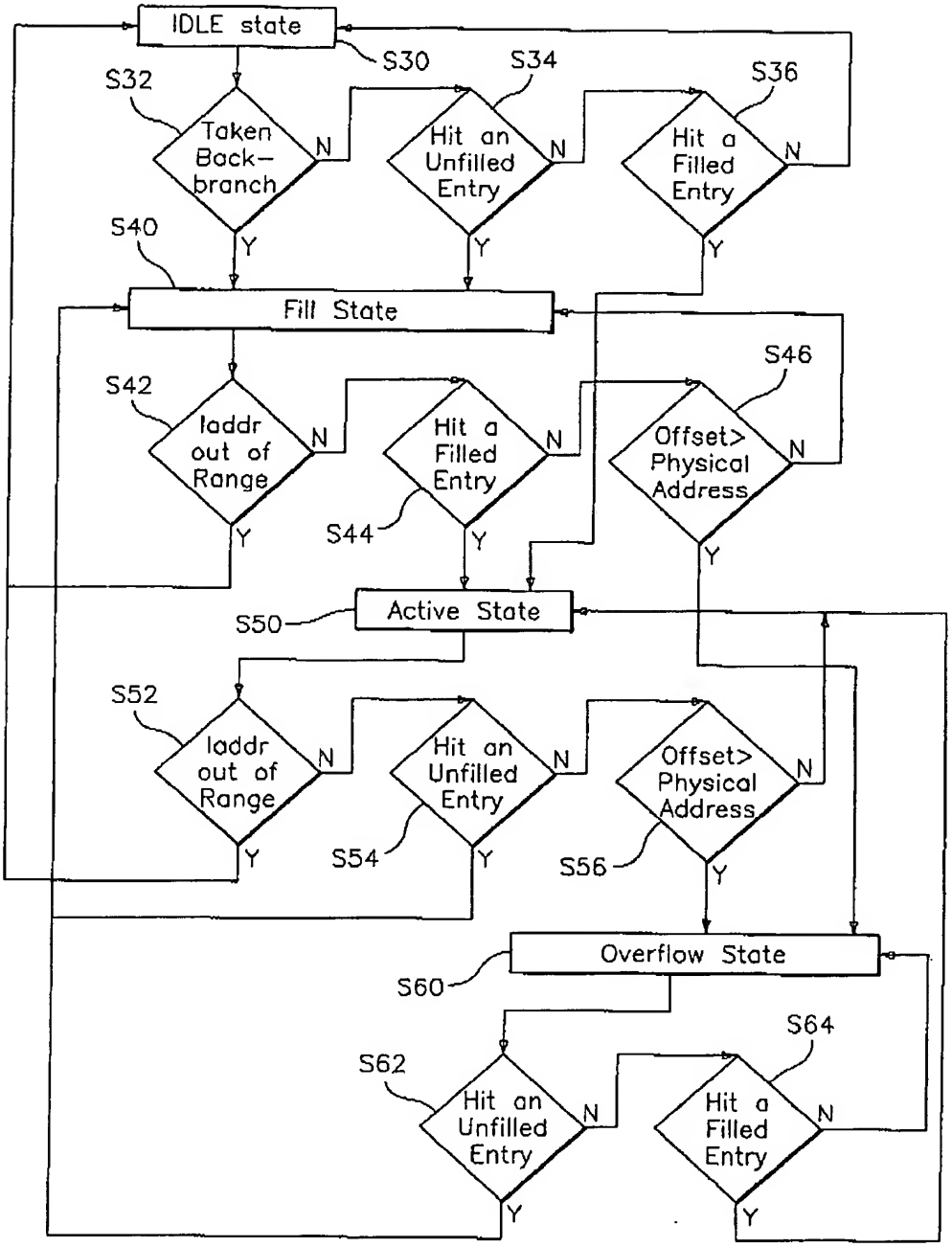
IDLE state
S30
S32
Taken Back-branch
N
Y
S34
Hit an Unfilled Entry
N
Y
S36
Hit a Filled Entry
N
Y
S40
Fill State
S42
laddr out of Range
N
Y
Hit a Filled Entry
N
S44
Y
S46
Offset> Physical Address
N
Y
S50
Active State
S52
laddr out of Range
N
Y
Hit an Unfilled Entry
N
S54
Y
Offset> Physical Address
N
S56
Y
Overflow State
S60
S62
Hit an Unfilled Entry
N
Y
S64
Hit a Filled Entry
N
Y

FIG. 4